

# 8 Pin SIL 5 Tap TTL Compatible Active Delay Lines

TAP DELAYS ±5% or ±2 nS†	TOTAL DELAYS ±5% or ±2 nS†	PART NUMBER	TAP DELAYS ±5% or ±2 nS†	TOTAL DELAYS ±5% or ±2 nS†	PART NUMBER
1.0 ± 0.5	*4 ± 0.5	EPA600-4	15	75	EPA600-75
1.5 ± 0.5	*6 ± 0.5	EPA600-6	20	100	EPA600-100
2.0 ± 1	*8 ± 1.0	EPA600-8	25	125	EPA600-125
2.5 ± 1	*10	EPA600-10	30	150	EPA600-150
3.0 ± 1	*12	EPA600-12	35	175	EPA600-175
4.0 ± 1.5	*16	EPA600-16	40	200	EPA600-200
5.0	*20	EPA600-20	50	250	EPA600-250
6.0	30	EPA600-30	60	300	EPA600-300
7.0	35	EPA600-35	70	350	EPA600-350
8.0	40	EPA600-40	80	400	EPA600-400
9.0	45	EPA600-45	90	450	EPA600-450
10.0	50	EPA600-50	100	500	EPA600-500
12.0	60	EPA600-60			

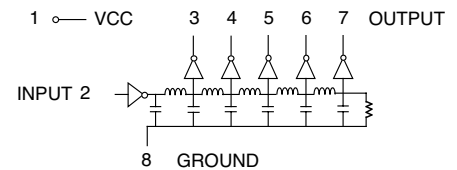
† Whichever is greater. Delay times referenced from input to leading edges at 25°C, 5.0V, with no load.

\* Delay times referenced from 1st tap

1st tap is the inherent delay: approx. 7 nS

DC Electrical Characteristics			Min	Max	Unit
Parameter	Test Conditions				
V <sub>OH</sub>	High-Level Output Voltage	V <sub>CC</sub> = min. V <sub>IL</sub> = max. I <sub>OH</sub> = max	2.7		V
V <sub>OL</sub>	Low-Level Output Voltage	V <sub>CC</sub> = min. V <sub>IH</sub> = min. I <sub>OL</sub> = max		0.5	V
V <sub>IK</sub>	Input Clamp Voltage	V <sub>CC</sub> = min. I <sub>I</sub> = I <sub>IK</sub>		-1.2V	V
I <sub>IH</sub>	High-Level Input Current	V <sub>CC</sub> = max. V <sub>IN</sub> = 2.7V		50	μA
		V <sub>CC</sub> = max. V <sub>IN</sub> = 5.25V		1.0	mA
I <sub>IL</sub>	Low-Level Input Current	V <sub>CC</sub> = max. V <sub>IN</sub> = 0.5V		-2	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = max. V <sub>OUT</sub> = 0. (One output at a time)	-40	-100	mA
I <sub>CC</sub> H	High-Level Supply Current	V <sub>CC</sub> = max. V <sub>IN</sub> = OPEN		115	mA
I <sub>CC</sub> L	Low-Level Supply Current	V <sub>CC</sub> = max. V <sub>IN</sub> = 0		115	mA
T <sub>RO</sub>	Output Rise Time	T <sub>d</sub> ≤ 500 nS (0.75 to 2.4 Volts)		4	nS
N <sub>H</sub>	Fanout High-Level Output	V <sub>CC</sub> = max. V <sub>OH</sub> = 2.7V		20 TTL LOAD	
N <sub>L</sub>	Fanout Low-Level Output	V <sub>CC</sub> = max. V <sub>OL</sub> = 0.5V		10 TTL LOAD	

## Schematic



Recommended Operating Conditions		Min	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.25	V
V <sub>IH</sub>	High-Level Input Voltage	2.0		V
V <sub>IL</sub>	Low-Level Input Voltage		0.8	V
I <sub>IK</sub>	Input Clamp Current		-18	mA
I <sub>OH</sub>	High-Level Output Current		-1.0	mA
I <sub>OL</sub>	Low-Level Output Current		20	mA
PW*	Pulse Width of Total Delay	40		%
d*	Duty Cycle		40	%
T <sub>A</sub>	Operating Free-Air Temperature	0	+70	°C

\* These two values are inter-dependent.

Input Pulse Test Conditions @ 25° C		Unit
E <sub>IN</sub>	Pulse Input Voltage	3.2 Volts
P <sub>W</sub>	Pulse Width % of Total Delay	110 %
T <sub>RI</sub>	Pulse Rise Time (0.75 - 2.4 Volts)	2.0 nS
P <sub>RR</sub>	Pulse Repetition Rate @ T <sub>d</sub> ≤ 200 nS	1.0 MHz
	Pulse Repetition Rate @ T <sub>d</sub> > 200 nS	100 KHz
V <sub>CC</sub>	Supply Voltage	5.0 Volts

## Package Dimensions

